B4 said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of address sizes is selected in response to a state of said second operating mode indication.

REMARKS

Claims 1-10 and 17-22 remain pending. In the present Office Action, claims 1-22 were provisionally rejected under the judicially-created doctrine of obviousness-type double patenting over U.S. Patent Application Serial No. 09/483,636 (the "copending application") in view of James L. Turley's Advanced 80386 Programming Techniques ("Turley"). Claims 1-5, 10, and 17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Turley. Claims 6-9, 11-16, and 18-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley in view of Khalidi et al., U.S. Patent No. 5,479,627 ("Khalidi"). Claims 1-7, 10-11, 14-19, and 21-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hammond in view of Intel. Claims 8-9, 12-13, and 20 rejected under 35 U.S.C. § 103(a) as being unpatentable over Hammond in view of Intel and further in view of Alpert. Applicants respectfully traverse these rejections and request reconsideration.

Turley, and Turley in view of Khalidi

Applicants respectfully submit that each of claims 1-10 and 17-22 recite combinations of features not taught or suggested in Turley, nor in Turley in view of Khalidi. For example, claim 1 recites a combination of features including: "a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication, a second operating mode indication, and one or more bits identifying a segment described by said segment descriptor as a code segment; a control register configured to store an enable indication, wherein said processor is configured to establish a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication".

The Office Action alleges that Turley teaches the segment descriptor. More particularly, the Office Action alleges that Turley teaches the first and second operating

mode indications at page 49, table: A segment descriptor; pages 47-48, paragraphs 5-2, page 50, Figure 2-2; page 51-52; page 53, paragraph 3; and page 54, table. With such general recitations of teachings, it is unclear exactly what in Turley's segment descriptor is alleged to be the first and second operating mode indications. However, the table labeled "A segment descriptor" on page 49 merely generally describes a segment descriptor, and offers no details. Page 47-48, paragraphs 5-2 generally indicate that segments have attributes, including what the segment is used for (code, data, stack) and privilege level. Additionally, this section generally indicates that a segment descriptor describes the segment. Figure 2-2 on page 50 is a diagram illustrating the contents of Turley's segment descriptor, which contents are described on pages 51-52.

More particularly, pages 51-52 contain a description of the type field and the S bit (System bit) shown in Figure 202. More particularly, the type field is described as "this 3-bit field indicates the type of segment you are defining. Common types are code, data, and stack." (Turley, page 51, paragraph 3). The S bit is described as "if this bit is clear, it indicates that this is a system segment descriptor. If it is set, this is a nonsystem (code, data, or stack) segment descriptor." (Turley, page 51, paragraph 4). Thus, Turley's type field and S bit, taken together, define a segment as being either system, code, data, or stack. Accordingly, Turley's type field and S bit cannot teach or suggest the first and second operating mode indications of claim 1: "a segment descriptor including a first operating mode indication, a second operating mode indication, and one or more bits identifying a segment described by said segment descriptor as a code segment".

Of the remaining information in Turley's segment descriptor, only the D bit appears to have anything to do with default address size (see Turley, page 52, paragraph 2). Turley only discusses the D bit as describing the default operand size, but Applicants believe that the 80386 uses the D bit for both address size and operand size (see e.g., Intel, page 11-13, paragraph 3). The D bit is described at page 3, paragraph 3 as well. However, the D bit alone cannot teach or suggest both a first operating mode indication and a second operating mode indication. See also the table on page 54 of Turley, which indicates that the size of operands within the segment is determined by 1 bit. Applicants

submit that 1 bit cannot teach or suggest both the first operating mode indication and the second operating mode indication.

Turley does not teach or suggest "a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication, a second operating mode indication, and one or more bits identifying a segment described by said segment descriptor as a code segment; a control register configured to store an enable indication, wherein said processor is configured to establish a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication". Khalidi is relied on to allegedly teach an address size larger than 32 bits. Khalidi does not appear to teach or suggest the above highlighted features, either. Accordingly, the combination of Turley and Khalidi does not teach or suggest the above highlighted features.

For at least the above-stated reasons, Applicants submit that claim 1 is patentable over Turley and Khalidi. Claims 2-10, being dependent from claim 1, are similarly patentable over Turley and Khalidi for at least the above stated reasons as well. Each of claims 2-10 recites additional combinations of features not taught or suggested in Turley and Khalidi.

Claim 17 recites a combination of features including: "establishing a default address size in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, said segment descriptor further including one or more bits identifying a segment described by said segment descriptor as a code segment". The teachings of Turley and Khalidi, highlighted above, similarly do not teach or suggest the above highlighted features of claim 17. Accordingly, Applicants submit that claim 17 is patentable over Turley and Khalidi for at least the above-stated reasons. Claims 18-22, being dependent from claim 17, are similarly patentable over Turley and Khalidi for at least the above stated reasons as well. Each of claims 18-22 recites additional combinations of features not taught or suggested in Turley and Khalidi.

Hammond in view of Intel, and further in view of Alpert

The rejection of claims 1-22 as being unpatentable over Hammond in view of Intel (and for some claims, further in view of Alpert) appears to be a reiteration of the rejection from the Office Action mailed September 24, 2002 (the "First Office Action") in the captioned application. Applicants submit that the arguments presented in the Response to the First Office Action (filed November 15, 2002) remain valid and incorporate those arguments by reference to preserve them for appeal. Essentially, Applicants argued that the First Office Action (and the present Office Action) have not met their burden of proving a *prima facie* case of obviousness because the combination of Intel and Hammond is not proper. Applicants reiterate that argument, and submit that it applies equally to claims 1-10 and 17-22, as amended. Applicants submit that the combination of Intel and Hammond as set forth in the First Office Action (and reiterated in the present Office Action) is not proper (for the reasons set forth in the previous response, and incorporated herein by reference), and thus cannot be used to reject claims 1-10 and 17-22 as originally filed, nor as amended. Applicants respond to the "Response to Remarks" section of the Office Action below.

In response to Applicants' argument that "it is unclear that the combination of Hammond and Intel, even if modified as suggested by the Office Action, would achieve the alleged advantage over a global mode flag, which would have to use an instruction cycle to change the flag setting before the instructions in the other operating modes could be executed", the Office Action states that the claim language does not refer to the number of instructions needed to change the flag setting nor the global mode flag. Applicants agree that the claim language does not refer to the number of instructions needed to change the flag setting or the global mode flag. Applicants were not arguing that the claims include such language, nor that the claimed invention achieves such an advantage. Instead, Applicants were illustrating why the Office Action has failed to establish the *prima facie* case of obviousness. The Office Action alleges that:

> moving the operating mode indicators to the segment descriptor would allow the operating mode to automatically vary depending on which selector is active and would be an advantage over a single global mode flag, which would have to use an instruction cycle to change the global mode setting before the instructions in the other operating mode could be executed. (present Office Action, page 21, lines 2-5 and First Office Action, page 16, lines 4-8).

Thus, the Office Action is alleging that modifying the teachings of Hammond and Intel to move the operating mode indicators to the segment descriptors would be obvious because an instruction cycle would be saved. Applicants have illustrated why this motivation is inaccurate:

> Applicants submit that Intel teaches the use of instructions to change the segment selectors in the segment registers. "Other segments can be used by loading their segment selectors into the segment registers" (Intel, page 3-10, third paragraph, last sentence). "More segments can be made available by loading their segment selectors into these register during program execution" (Intel, page 11-9, first paragraph, last sentence). "There are forms of the MOV instruction to load the visible part of these segment registers [the segment selector, in Figure 11-6]. The invisible part is loaded by the processor" (Intel, page 11-9, second paragraph, last two sentences). Since instructions are used to change the segment selectors in Intel, it would appear that the alleged advantage over a global flag is not achieved *by the proposed modification*.

The present Office Action has not overcome this deficiency in the motivation to perform the modification. The present Office Action alleges:

> Intel does have an advantage to this, because Intel's system uses one instruction that combines loading the segment register and the segment/mode flag value instruction. Therefore, Intel would use only one instruction cycle and not require the extra instruction cycle suggested by Applicants' argument. (present Office Action, page 30, lines 15-19)

Applicants respectfully disagree with the above statement. It is unclear what is meant by the "segment/mode flag value instruction". However, prior to the proposed modification, as the Office Action states, an instruction cycle would be required to change the global mode flag. If the global mode flag were moved to segment descriptor, an instruction (a

segment load instruction) would be required to change the global mode flag (by loading a new segment descriptor). Thus, no instruction cycle has been saved. Furthermore, additional instructions would be required to write the desired global mode flag into the segment descriptor. Thus, it would appear that more instructions may be required with the proposed modification. For at least these reasons, Applicants submit that the motivation to make the modification is in error, and thus a *prima facie* case of obviousness has not been established.

In response to Applicants' argument that Intel teaches away from the proposed modification, the Office Action states that "combining two references does not mean combining their specific structures but what each structures suggests and what combining the two structures suggests to one of ordinary skill in the art" (present Office Action, page 30, lines 20-22). Applicants are not arguing the combination in this case, but the proposed modification to the combination. The combination, alone, teaches a global mode flag in a register and a D/B bit in the segment descriptor, which fails to teach or suggest the features of claims 1 and 17. The First Office Action then modifies the combination to move the global mode flag into the segment descriptor. It is this modification that Intel teaches away from, by reserving the only available bit in the segment descriptor and requiring that it be set to zero. One of skill in the art would not be motivated to overcome this clear teaching away, especially since the proposed motivation is inaccurate, as pointed about above.

In response to Applicants' argument that Hammond and Intel do not teach or suggest "a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor" as recited in claim 17, the Office Action alleges that "It does not matter whether the mode indicators are in the control register or the segment descriptor because it still functions the same. There is only a shifting of parts from the control register to the segment register. See, *In re Japiske*" (present Office Action, page 32, lines 2-5). Applicants respectfully disagree that *In re Japiske* applies to claim 17. *In re Japiske* states that claims to a hydraulic power press which read on the prior art except with regard to the position of the start switch were held

unpatentable because shifting the position of the start switch would not have modified the operation of the device. However, the differences between the alleged combination and claim 17 would result in different operation (e.g., in how the indications are changed, as highlighted above). "The mere fact that a worker in the art could rearrange the parts of the reference to meet the terms of the claims...is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device" *Ex part Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984). (Emphasis added). As highlighted above, the prior art fails to provide such motivation.

In response to Applicants' argument that there is no teaching or suggestion in Hammond or Intel to make the modification proposed by the Office Action, and that there is no evidence that generally available knowledge in the art that provides the motivation for the modification, the Office Action states that "the references do not have to specifically teach the proposed modifications nor does the suggestion to combine prior art teachings have to be found in a specific reference". Applicants do not dispute this statement, but respectfully submit that no motivation has been properly provided. Applicants refuted the motivation alleged by the First Office Action in subsequent paragraphs of the argument presented in the previous response, and in the arguments above related to the Response to Remarks section of the present Office Action. Thus, some other motivation must be proved if the rejection is to stand. That motivation must be found either in the references or in generally available knowledge of those skilled in the art. The Office Action has provided neither. Similarly, Applicants disagree with the statement that the hindsight used in the Office Action is permissible because it "takes into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made" (present Office Action, page 30, lines 6-7). Applicants have explained in the previous response and above why only knowledge which was within the level of ordinary skill in the art at the time the invention was made does not teach or suggest the claims, and thus the hindsight is impermissible.

Comments re: *In re Rose*

The Office Action frequently cites *In re Rose*, 220 F.2d 459, to support the rejection of various claims that recite numerical operand and/or address sizes. The rejections use *In re Rose* to allegedly support the general statement that "size does not matter".

Applicants note that *In re Rose* refers to the size issue only briefly, stating "We do not feel that this limitation is patentably significant since it at most relates to the size of the article under consideration which is not ordinarily a matter of invention. *In re Yount*, 171 F.2d 317" *In re Rose* at 463. Thus, *In re Rose* does not stand for the general proposition that "size does not matter", but rather says that it is not ordinarily a matter of invention, relying on *In re Yount* without providing any further illumination. That is, size may matter in some circumstances, but *In re Rose* does not provide any illumination as to what those circumstances would be.

In re Yount refers to *In re Kirke*, 40 F.2d 765, for the proposition that size is not ordinarily a matter of invention (*In re Yount* at 318). However, in *In re Yount*, Yount was arguing that his claimed bags were of extremely large size. Yount had, in his own specification, indicated that large and small bags were equivalent. Yount's admissions thus could not support an argument that large bags were patentable over anticipatory teachings related to small bags. Applicants submit that the facts of *In re Yount* do not apply.

In re Kirke states that "there is nothing patentable in making a machine or apparatus larger or smaller, if it produces the same result in the same manner" (*In re Kirke* at 767. *In re Kirke* was related to a boiler for using waste heat from furnaces, kilns, etc. in the generation of steam. At issue was the limitation that the tubes in the boiler be at least 50 times as long as their diameters. However, there was prior art of record in the application which showed this limitation in smaller boilers. Additionally, the prior art stated that the same limitation could be used in larger boilers. These facts do not support the general conclusion that size never matters, but that size does not matter if the same

result is produced in the same manner. The numerical operand size and address sizes recited in various claims do not produce the same result in the same manner...addresses and/or results having differing numbers of bits are the result.

In re Kirke also states "What does or does not constitute invention is incapable of exact definition. Each case depends largely on its own facts" (*In re Kirke* at 765). Thus, the line of cases on which *In re Rose* rests requires a consideration of the facts in an individual case, and should not be used to support the general statement that "size does not matter".

Double Patenting

Applicants respectfully disagree with the double patenting rejection, at least with respect to some of the claims. However, Applicants respectfully request that the double patenting rejection be held in abeyance until the claims are otherwise indicated as allowable, at which time Applicants will consider the filing of a terminal disclaimer (or, if the copending application has not been allowed, Applicants will request cancellation of the provisional double patenting rejection -- See MPEP 804(I)(B), second and third paragraphs, regarding withdrawing the provisional double patenting rejection and allowing a case to issue if there are no other outstanding rejections).

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-54700/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☒ Marked-up Copy of Amended Claims

☐ Marked-up Copy of Amended Paragraphs

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,

Lawrence J. Merkel
Reg. No. 41,191
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: 3/4/03

Marked-up Copy of Amended Claims:

1. (Amended) A processor comprising:

a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication, [and] a second operating mode indication, and one or more bits identifying a segment described by said segment descriptor as a code segment;

a control register configured to store an enable indication, wherein said processor is configured to establish [an operating mode] a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication.

2. (Amended) The processor as recited in claim 1 wherein said [operating mode] default address size is a first [operating mode] address size if said enable indication is in an enabled state and said first operating mode indication is in a first state, and wherein said [operating mode] default address size is a second [operating mode] address size if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state.

3. (Amended) The processor as recited in claim 2 wherein said second [operating mode] address size is one of a plurality of [operating modes] address sizes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of [operating modes] address sizes is selected in response to a state of said second operating mode indication.

4. (Amended) The processor as recited in claim 3 wherein one of said plurality of [operating modes] address sizes is a 32 bit [operating mode] address size.

5. (Amended) The processor as recited in claim 3 wherein one of said plurality of

[operating modes] address sizes is a 16 bit [operating mode] address size.

6. (Amended) The processor as recited in claim 2 wherein said first [operating mode includes a default] address size [which] is greater than 32 bits.

10. (Amended) The processor as recited in claim 1 wherein, if said enable indication is in a disabled state, said first operating mode indication is undefined and said processor is configured to establish said [operating mode] default address size responsive to said second operating mode indication.

17. (Amended) A method comprising:

establishing [an operating mode] a default address size in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, said segment descriptor further including one or more bits identifying a segment described by said segment descriptor as a code segment; and

[fetching operands and] generating addresses of said default address size [in response to said operating mode].

18. (Amended) The method as recited in claim 17 wherein said establishing comprises establishing a first [operating mode] address size responsive to said enable indication being in an enabled state and said first operating mode indication being in a first state, and wherein said first [operating mode includes a default] address size is greater than 32 bits.

21. (Twice Amended) The method as recited in claim 18 wherein said establishing further comprises establishing a second [operating mode] address size responsive to said enable indication being in an enabled state, said first operating mode indication being in a

second state, and said second operating mode indication being in said first state, and wherein said second [operating mode includes a default] address size [of] is 32 bits.

22. (Amended) The method as recited in claim 18 wherein said establishing further comprises establishing one of a plurality of [operating modes] address sizes if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of [operating modes] address sizes is selected in response to a state of said second operating mode indication.